Alessandro Cilardo

Associate Professor
Department of Electrical Engineering and Information Technologies
University of Naples Federico II
via Claudio 21, 80125 Napoli
Email: acilardo@unina.it
Tel: +39 333 6974250

Resumé

Alessandro Cilardo is currently an Associate Professor (*Professore Associato*) affiliated with the University of Naples Federico II, Research/Teaching Sector (*SSD*): ING-INF/05 Information Processing Systems (*Sistemi per l'Elaborazione dell'Informazione*). He graduated in Electronics Engineering in 2003 and received a PhD degree in Computer Science in 2006 from the University of Naples Federico II.

Alessandro Cilardo's research activity focuses on high-performance computing architectures, digital design methodologies, security applications, and on-chip networks. He is the single or main author of numerous peer-reviewed papers published in leading scientific journals and conferences, such as IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Industrial Informatics, ACM Transactions on Architecture and Code Optimization, ACM Transactions on Embedded Systems, IEEE Transactions on Circuits and Systems-I, The Proceedings of the IEEE, IEEE Transactions on Information Forensics & Security, IEEE/IET Electronics Letters, DATE, VLSI-SoC, FPL, ITC conferences, and others.

He received a number of acknowledgments including the Intel HARP grant, the Altera Innovate Europe SoC Award 2015, the MBDA Innovation Award, the Simagine and eGate awards sponsored by Gemalto for innovative Smart Card applications. Earlier in his career, he received the 2003 Federcomin-AICA Award for the best thesis in Italy in the field of Information and Communication Technology.

He is involved in a number of research projects at both the national level (PRIN and STAR projects) and the European level (FP7 and H2020 projects) in addition to a number of projects and contracts with industry.

He is currently serving as an Associated Editor for top rank international journals, including IEEE *Transactions on Circuits and Systems I: Regular Papers*, IEEE *Transactions on Circuits and Systems II: Express Briefs*, as well as Elsevier *Microprocessors and Microsystems: Embedded Hardware Design*, and Wiley/Hindawi *Security and Communication Networks*.

He served as an expert/reviewer for several national and international funding agencies, including the European Research Executive Agency (REA) in the framework of the H2020 programme. He also served as a chair/TPC member for numerous conferences and as a reviewer for a large number of scientific journals and conferences, including many IEEE and ACM transactions.

He is a Senior Member of the IEEE, a member of the IEEE Industrial Society, and a member of the High Performance and Embedded Architectures and Compilation (HiPEAC) network of excellence.

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Research

Leadership of funded research projects

- 2015–2018: Unit leader for the Centro Regionale Information Communication Technology (CeRICT) s.c.r.l. within the **Horizon 2020** project MANGO: *exploring Manycore Architectures for Next-GeneratiOn HPC systems*, project ID: 671668, H2020-FETHPC-2014 competitive call. Among other duties, Alessandro Cilardo is WP leader for CeRICT in WP3 "Architecture Exploration for Real-Time HPC".
- 2018–2021: Unit leader for the Centro Regionale Information Communication Technology (CeRICT) s.c.r.l. within the **Horizon 2020** project RECIPE: *REliable power and time-ConstraInts-aware Predictive management of heterogeneous Exascale systems*, project ID: 801137, H2020-FETHPC-2017 competitive call.
- 2016–2020: Coordinator Contact for the **Horizon 2020** project NASDAC: *iNnovative Approaches for Scalable Data Assimilation in oCeanography*, project ID: 691184, MSCA-RISE-2015 competitive call (coordinator: University of Naples Federico II).
- 2019–2022 Unit leader ("*Responsabile dell'Unità di Ricerca*") for the University of Naples Federico II within the project SPHERE: *Software architecture for Predictable HEterogeneous REal-time systems*, funded in the framework of the Programmi di Ricerca Scientifica di Rilevante Interesse Nazionale (**PRIN**) programme.
- 2014–2016: Principal Investigator of the project HtComp: *Heterogeneous Computing in The Cloud: Enabling Tomorrow's High-Performance Applications*, within the call Programma Sostegno Territoriale alle Attività di Ricerca (STAR) - Linea d'intervento 1: Junior Principal Investigator Grants, 2014-2016. The programme is cofunded by Compagnia San Paolo, it relies on a very selective evaluation process, carried out by an independent body (the European Science Foundation, **ESF**), and it is aimed at selecting research projects with a high potential for European funding calls. The project has fostered the technical and networking activities that led to the H2020 proposal MANGO, then approved for funding by the European Community in November 2014.

- 2019–2021: Local Principal Investigator for the international collaboration project *Approximate Computing Techniques for Resource Constrained Edge Devices*, in the framework of the Scheme for Promotion of Academic and Research Collaboration (SPARC) programme, funded by the Indian Institute of Technology.
- 2016–2017: Principal Investigator of project "Methodologies for hardware/software co-design oriented to next-generation Silicon technologies", accepted for funding ex L.R. 5/2002 call, D.D. 134 Mar 11, Campania Region, 2010.
- 2016 –2017: Principal Investigator of project "Approcci di modellazione multi-paradigma per lo sviluppo di sistemi embedded in ambito automotive con requisiti di affidabilità", accepted for funding ex. L.R. 5/2002 call, D.D. n. 59 Dec 23, Campania Region, 2013.
- 2010: Grant for the proposal "A HPC application for collision search in cryptographic hash functions" (Application ID: 253) within the Capacities Area/Research Infrastructures HPC-EUROPA2 European project, ID: 228398.
- 2012: Grant for the proposal "Evaluating GPU-based solutions for HPC collision search in cryptographic hash functions" (Application ID: 1268) within the Capacities Area/Research Infrastructures HPC-EUROPA2 European project, ID: 228398.

Editorial activities

- 2016–present: **Associate Editor** of IEEE *Transactions on Circuits and Systems I: Regular Papers* (TCAS-I), the flagship journal of the IEEE Circuits and Systems Society (**Q1** according to ISI Ranking, **top 10%** according to Scopus).
- 2016–2018: **Associate Editor** of IEEE *Transactions on Circuits and Systems II: Express Briefs* (TCAS-II).
- **Editorial Board member** of *Elsevier Microprocessors and Microsystems: Embedded Hardware Design* (MICPRO).
- 2016–present: **Associate Editor** of the Wiley/Hindawi *Security and Communication Network* journal.
- 2015: **Guest Editor** for the Hindawi *Mobile Information Systems* journal.

Memberships

- 2015–present: *Senior Member* of the Institute of Electrical and Electronics Engineers (IEEE). This grade of membership is held by less than 8% of the IEEE members. The recognition is bestowed upon members with at least 10 years of professional experience, at least five years of significant research performance in terms of technical contribution and professional leadership, and endorsement by at least three IEEE Fellows or Senior Members.
- 2016–present: Member of the IEEE Industrial Society.
- 2015–present: Member the *High Performance and Embedded Architecture and Compilation* (HIPEAC) European network of excellence.

Participation in scientific projects as a team member

Alessandro Cilardo served as a team member in a number of national and European research projects, including:

- European **FP7** project FP7-ARTEMIS-2012-1 "CRYSTAL Critical System Engineering Acceleration", project ID: 332830
- National research project: **PRIN** 2005 "COMMUTA: Hardware/software mutant components for distributed, dynamically reconfigurable systems".
- National research project: **PRIN** 2010-2011 "TENACE: Protecting National Critical Infrastructures From Cyber Threats", funded by the Italian Education and Research Ministry ex D.D. n. 719, Oct. 23, 2012.

- Regional research project POR Campania FESR 2007-2013 - O.O. 2.2 “Progetto Metadistretto del Settore ICT – SIINTEGRA”.
- Regional research project POR Campania FESR 2007-2013 - O.O. 2.2 “Progetto Metadistretto del Settore ICT - Sistema di comunicazione per l'integrazione delle informazioni nella distribuzione commerciale e nei punti vendita”.
- Regional research project POR Campania FESR 2007-2013 - O.O. 2.2 “Progetto Metadistretto del Settore ICT – RADIONET”.
- MASSIF: Management of Security Information and events in Service InFrastructures, FP7-ICT European Integrated Project, Project ID: 257475.
- Research project: P.O.N. “Ricerca e Competitività 2007-2013 - Azione II - Progetto IESWECAN”. Code: PON01_01516.
- Research project: “Ricerca e Competitività 2007-2013 - Tecnologie innovative per la SICURezza della circolazione dei veicoli FERroviari” (SICURFER), P.O.N., funded by the Italian Education and Research Ministry, ex D.D. n. 1, Jan. 18, 2010, Code: PON01_00142
- Research project: “Ricerca e Competitività 2007-2013 Asse I, “Smart Health - Cluster OSDH - Smart FSE – Staywell”, P.O.N., D.D. n.283, Feb. 2, 2013, Code: PON04a2_C.

International collaborations

- 2010–2012: HPC access grantee and visiting scholar at the Barcelona Supercomputing Center, also including activities funded by the HPC-Europa2 project
  (https://www.bsc.es/annual-report/2014/INDEX_PHP/PEOPLE_OF_THE_BSC_CNS.HTM)
- 2015–present: Cooperation with the Argonne National Laboratory, US, within the MSCA project “NASDAC: iNnovative Approaches for Scalable Data Assimilation in oCeanography”.
- 2014: Visiting scholar at Universitat Politècnica de València (UPV).
- 2014: Visiting scholar at Imperial College London.
- 2014–present: Promoter of an Erasmus exchange with the Technische Universität Dresden, Germany.
- 2014–present: Promoter of an Erasmus exchange with the Universidad Politécnica de Madrid, Facultad de informática, Spain.
- 2015–present: Promoter of an Erasmus exchange with the Universitat Politècnica de València, Escuela Técnica Superior de Ingeniería Informática (ETSINF), Spain.

Participation in evaluation committees of funding agencies

Alessandro Cilardo has served as an expert/evaluator for a number of national and international funding agencies:

- 2017: Appointment by the European Research Executive Agency (**REA**) as an expert for evaluating project proposals in the context of the **Horizon 2020** *Digital Security LEIT-2017* call
- 2011–2020: Reviewer for the Executive Agency for Higher Education, Research, Development and Innovation Funding (**UEFISCDI**) for the evaluation of research project proposals
- 2018: Reviewer for the Czech Science Foundation for the evaluation of research project proposals
- 2016: Reviewer/Rapporteur for the Ministero dell’Istruzione, dell’Università e della Ricerca (**MIUR**) for the evaluation of project proposals within the *Progetti di Ricerca di Interesse Nazionale* (PRIN) programme.
- 2015: Referee for the Università degli Studi dell'Insubria within a competitive call for proposals aimed at funding a research fellowship.
- 2014–2015: Reviewer for the Ministero dell’Istruzione, dell’Università e della Ricerca (**MIUR**) for the evaluation of project proposals within the *SIR* programme (preselection).

- 2012–2013: Reviewer for the Ministero dell'Istruzione, dell'Università e della Ricerca (**MIUR**) for the evaluation of project proposals within the *Futuro in Ricerca* 2012 programme (preselection).
- 2007: Reviewer for the Canadian programme SHARCNET: *Research Support Programmes: Fellowships & Dedicated Resources*.

Organization of international conferences

Since 2003, Alessandro Cilardo has participated in a number of international conferences and workshops as a track chair, technical program committee (TPC) member, invited speaker, panelist, session chair, reviewer, and author/speaker. The conferences attended as a speaker include DATE (12 papers accepted and presented up to 2019), FPL, HPCC, DSD, VLSI-SoC, ICESS, 3PGCIC, ITC, PDP, etc. The following list only includes the most recent and relevant activities.

- 2018: **Program Chair** of the 3rd International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS).
- 2018: **Track chair** of the 13th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era, "Integrated Systems Design" track.
- 2016: **Track chair** of the 11th International Conference on P2P, Parallel, Grid, Cloud and Internet Computing (3PGCIC), "Heterogeneous High-Performance Architectures and Systems" track.
- 2014: **Chair** of the 2014 Workshop on "Electronic System-Level design towards Heterogeneous computing", within the Design Automation and Test in Europe (DATE) 2014 conference.
- 2015: **Track chair** of the 2015 IEEE International Conference on Embedded Software and Systems, track "Systems, Models and Algorithms".
- 2016–2019: **Technical program committee** member of the Design Automation and Test in Europe (DATE), one of the most important and selective venues in the area of digital design, "Reconfigurable Computing" track.
- 2015–2016: **Technical program committee** member of the "Workshop on Cryptography and Security in Computing Systems (CS2)" 2016.
- 2012–2013: **Technical program committee** member of the "IEEE International Conference on Advanced Information Networking and Applications (AINA) 2013".
- 2016–2019: **Technical program committee** member of the "International Workshop on Big Data Processing in Online Social Network (BOSON) 2016".
- 2016–present: **Technical program committee** member of the "Workshop on Cryptography and Security in Computing Systems (CS2)" 2017.
- 2015–2016: **Technical program committee** member of the "6th International Workshop on Polyhedral Compilation Techniques IMPACT 2016".
- 2014: **Technical program committee** member of the "International Workshop on Cloud and Distributed System Applications (CADSA) 2014".
- 2016–2019: **Technical program committee** member of the "IEEE Conference on Dependable and Secure Computing", "Track #2: System Electronics, VLSI, and CAD".
- 2016–present: **Technical program committee** member of the "Euromicro Conference on Digital System Design (DSD) 2017".
- 2016–2018: **Technical program committee** member of the "CompHPC 2017 International Conference on Computational Methods and Algorithms on HPC Platforms and Accelerators".
- 2016: **Session Chair** of the Reconfigurable Computing session during the *Design Automation and Test in Europe* (DATE) 2016 conference.
- 2017: **Technical program committee** member of the "IEEE Conference on Dependable and Secure Computing".

Invited talks

- June 28, 2019 – Invited talk: "At the foundation of cybersecurity: can we *trust* today's processing technologies?", within the *Security and Data Flows in the European Union* roundtable, Fondazione Bruno Kessler on June 28-29, Trento, Italy.
- May 18, 2017 – Invited talk on "MANGO: implications and contributions to Extreme-Scale Demonstrators", EsD roundtable@ European HPC Summit Week, Barcelona, Catalunya.
- Jan 24, 2017 – Panelist and invited presentation on the H2020 European Project MANGO, during the "Power-Efficient GPU and heterogeneous Multi-/Many-core Computing Workshop" within the *High Performance and Embedded Architecture and Compilation* (HIPEAC) Conference.
- Aug 25, 2015 – Invited Talk on "Customizable Heterogeneous Acceleration for Tomorrow's High-Performance Computing", given within the 12th IEEE *International Conference on Embedded Software and Systems* (ICESS), New York, 24-26 Agosto 2015.
- Sept 21, 2015 – Invited Talk on "Reconfigurability in HPC: opportunities and challenges", given during the High Performance and Embedded Architecture and Compilation (HIPEAC) *Computing System Week* (CSW), Milano, Italy.
- Mar 28, 2014 – Invited Talk on "Borrowing high-level paradigms from parallel computing: An OpenMP-based design flow", given during the Special Interest Workshop W3 within the *Design Automation and Test in Europe* (DATE) conference.
- Jan 19, 2016 – Session chair and panelist on High-Level Synthesis during the 6th *International Workshop on Polyhedral Compilation Techniques* (IMPACT) 2016.
- Dec 2, 2016 – Presentation on "Harnessing the FPGA potential through GPU-like programming", H2020 Info Day on ICT 5 Customised and low energy computing, European Commission Auditorium, Brussels.
- Apr 21, 2017– Invited Talk on "The nu+ LLVM backend", LLVM Social - Italy, DEIB, Politecnico di Milano.

Awards and acknowledgements

Since 2004, Alessandro Cilardo has received a number of industrial awards for applied research activities as well as academic acknowledgements for scientific results, including:

- 2016: Grant received from **Intel Corporation** within the Intel Hardware Accelerator Research Program, for the project "nu+: Harnessing the FPGA potential through GPU-like programming". The grant, assigned to 30 research centers worldwide according to the **HARP** v.2 call, provides early access to next-generation Intel CPU+FPGA (Broadwell + Arria10) platforms for experimental purposes.
- 2016: Acknowledgment for a *highly cited work* on Elsevier Journal of Systems Architecture (JSA): A. Cilardo, L Gallo, N. Mazzocca, "Design space exploration for high-level synthesis of multi-threaded applications", Journal of Systems Architecture, vol. 59, no. 10, pp. 1171-1183, 2013.
- 2015: Winner of the **Innovate Europe award**, SoC category, for a project entitled "FPGA in the Cloud: Reconfigurable Technologies Boosting Homomorphic Encryption", sponsored by ALTERA, now part of Intel Corporation, a worldwide leading FPGA manufacturer. The award ceremony was hosted by the Field Programmable Logic (FPL) conference at the Royal Institution, London, UK, September 2015.
- 2011: **MBDA Innovation Award**, assigned by MBDA to internal activities having the highest innovation impact. The activity was part of a contract coordinated by Alessandro Cilardo with MBDA dealing with an embedded controller of a radar antenna.
- 2006 and 2008: **Simagine Award**: acknowledgments achieved by projects proposed by Alessandro Cilardo based on innovative mobile technologies, such as Near-Field Communication (NFC), still unexplored at the time. The applications were awarded out of a large number of proposals (100 to 300, depending on the edition) by a committee of experts coordinated by Gemalto (former Axalto), the French leader company in smart card manufacturing. The developed prototypes were presented during the Mobile World Congress in Barcelona.

- 2005: **eGate Award** assigned by Axalto for an innovative application based on USB-enabled smartcard devices. The prototype demonstration and the award ceremony took place during the JavaOne conference in San Francisco, USA, in 2005.
- 2005 and 2004: Grants from the European Design and Automation Association (**EDAA**) supporting the participation at the DATE 2005 and DATE 2004 conferences, respectively.
- 2004: **Federcomin-AICA Award** for the best thesis in Italy in the field of Information and Communication Technology (currently known as AICA-Confindustria award).

Technological transfer

- 2013–2014: Principal Investigator of a research contract with Ansaldo STS S.p.A. dealing with the Development of methodologies for verification and validation of critical systems using model-based approaches, granted by Ansaldo STS S.p.A. in the framework of European project FP7-JTI-ARTEMIS-2010 "MBAT: Combined Model-based Analysis and Testing of Embedded Systems", project ID: 269335.
- 2008–2009: Principal Investigator of a research contract between STMicroelectronics and the Dipartimento di Informatica e Sistemistica, dealing with Implications of the IEC 61508 standard for Systems-on-Chip.
- 2015–2018: Principal Investigator of a research contract between DIETI and the Centro Regionale Information Communication Technology (CeRICT) s.c.r.l., for the participation of the Università degli Studi di Napoli Federico II as a CeRICT linked third party within the Horizon 2020 project MANGO, as per Grant Agreement n. 671668, European Commission, H2020-FETHPC-2014 competitive call.
- 2015–2015: Principal Investigator of a research contract with the Centro Italiano Ricerche Aerospaziali (CIRA) s.c.p.a. dealing with Technological transfer of technologies, design methodologies, and development tools for hardware-reconfigurable systems.
- 2009–2012: Principal Investigator of four research contracts between MBDA Italia S.p.A. and the Consorzio Inter-universitario Nazionale per l'Informatica (CINI) dealing with the development and evaluation of innovative techniques for embedded control firmware in frontal antennas.
- 2013: Principal Investigator of a research contract between Akron B.T. srl and the Consorzio Inter-universitario Nazionale per l'Informatica (CINI) dealing with the design and implementation of an innovative cryptographic system for protocol-based secure data transmission through untrusted channels including public networks.
- 2021: Principal Investigator of a research contract between Prometeon Tyre Group and the Department of Electrical Engineering and Information Technologies, dealing with embedded system design for real-time data acquisition and processing.